Accelerated Switching Function Model of Hybrid MMCs for HVDC System Simulation

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Abstract: An accelerated switching function model (SFM) of the hybrid modular multilevel converter comprising both full-bridge (FB) and half-bridge (HB) submodules (SMs) in each arm is presented for HVDC system simulation, where auxiliary circuits are adopted to represent all possible current paths during normal and fault conditions. The proposed SFM can represent the negative voltage generating capability of the FB SMs and the equivalent switching functions in the blocking states of the FB and HB SMs are also introduced in the proposed model to accurately replicate the potential charging of the SM capacitors, yielding improved simulation accuracy compared to other alternatives. In addition to the faster simulation speed, the proposed model accurately reproduces the converter behaviour during various operating conditions, including normal operation, AC fault, and DC fault, etc. The proposed SFMs are assessed in MATLAB/Simulink environment using both down- and full-scale HVDC links and the simulation results confirm the validity of the proposed model in terms of model accuracy and improved simulation speed.

1. Introduction

As modular multilevel converters (MMCs) typically use hundreds of submodules (SMs) per arm in HVDC application, it is extremely time consuming to simulate the whole system using detailed switching models (DSMs). To reduce computation time and accelerate the simulation speed, the average model (AM) [1, 2] and the accelerated SM level model [3, 4] have been researched extensively to evaluate MMC performance in normal operation and during faults.

In [1, 5], each arm of the MMC is represented by a controllable voltage source, coupled with a series connection of a controlled current source and a DC capacitor. Such an average model provides adequate representation of the MMC behaviour seen by the external circuits under normal operation. However, the current paths during DC faults are not provided. In order to represent the response of the MMC during faults, ideal switches and a thyristor are introduced into the average value model in [6]. All the converter SM capacitors are equivalent to one DC capacitor, which is disconnected from the DC side during a DC fault. As a result, the charging of the DC capacitors in the arms by the fault current following the blocking of the MMC cannot be represented, resulting in significant errors.

In [2], additional switches and diodes are added to the average model to consider the influence of the lumped DC capacitor and the unidirectional characteristics of the freewheeling arm currents during a fault. However, such model is only valid when the SM capacitance is large enough to maintain near constant SM capacitor voltages. In [7], a modified average model using six capacitors (one for each arm) and additional auxiliary circuit was developed to provide an improved representation of the MMC behaviour during various operating conditions, including AC and DC fault scenarios.

To represent the detailed behaviour of individual SM, SM level models are proposed to reproduce the capacitor voltage of each SM. The SM level model based on Thevenin equivalents is introduced in [8] and significantly accelerates the simulation speed compared to DSMs without compromising the accuracy for MMC normal operation. But it is unsuitable for fault studies due to the lack of the representation of the fault current paths after the converters are blocked.

The off-state IGBT is simplified as an open circuit in [3], and thus the calculations of the current and voltage divisions, required in [8], are avoided, yielding faster simulation speed. In addition, the adopted fault current path makes it capable of representing MMC behaviour during a DC fault. However, as the equivalent switching function in the blocking state of the converter is not considered, the potential charging of the half-bridge (HB) SM capacitors by the positive fault current (from the top to the bottom) cannot be represented.

Reference [9] further improves the accuracy of the SM level model by considering the different internal resistances and threshold voltages of the IGBTs and the anti-parallel diodes. The blocking of the MMC after a fault is represented by opening the ideal switch, which is connected in series with the controlled voltage source in each arm. As a result, the fault current cannot flow through the arm from the top to the bottom after the converter is blocked, resulting in simulation errors.

The model proposed in [10] replaces the ideal switches in [9] with diodes and thus it can represent the possible current paths of HB SM based MMC. However, two controlled sources are required to represent the voltage generated by the HB SMs in each arm under normal operation and in blocking state and have to be switched at different operating conditions, which complicates the model. In addition, the characteristic differences between the IGBTs and diodes, including the threshold voltages, are not considered either.

Aforementioned average models and SM level models have been used for the study of the generic MMC based on HB SMs, which do not have the DC fault blocking capability. Another alternative is the full-bridge (FB) SMs and MMCs with FB SMs can block DC faults and offer greater controllability. By combing FB and HB SMs in each arm, the hybrid MMC can block DC faults with reduced losses and

capital costs compared to the MMC composed of only FB SMs. The Alternate Arm Converter (AAC) has the DC fault blocking capability and requires fewer SMs with reduced capacitance. With short-overlap operation, AAC is conventionally operated on 'sweet spot', where the AC voltage peak is 27% higher than the DC voltage, in order to balance the AC and DC side energies. This limits the AC voltage flexibility [11]. Extended overlap operation of AAC is proposed in [11-13] to tackle this issue and to eliminate any potential 6th harmonic in the DC current [11, 14-16]. However, this leads to higher AC terminal to ground voltage stress [12]. In addition, the direct switches in the AAC arm require series connection of large numbers of IGBTs. The MMC based on clamp double (CD) SMs [17, 18] can also block the DC fault. It has lower power losses and required semiconductor number comparted to FB MMCs but higher than that of the hybrid MMC, as discussed in [19]. The hybrid MMC has been under extensive research [20, 21] and is thus considered in this paper.

The average model of the hybrid MMC is proposed in [22], which can reproduce the converter behaviour during normal operation and the DC fault blocking capability of the FB SM in the event of a DC fault. However, due to the shoot-through of the diodes, the model cannot replicate the negative voltage generating capability of the FB SMs when the hybrid MMC is actively controlled. By rearranging the two voltage sources and using the series connection of the ideal switches and diodes, the model for the FB stack proposed in [10] is capable of reproducing the negative voltage generating capability. However, as previously described, two controlled voltage sources are required.

Compared to the aforementioned pure numerical simulation, hardware-in-the-loop (HIL) test significantly accelerates the simulation speed and provides an attractive tool for the real-time simulation of MMCs. Test benches, however, are required and have to be carefully designed to provide sufficient accuracy and run the simulation in real-time [23].

The aim of this study is to develop an improved SM level switching function model (SFM) for the hybrid MMC with improved simulation speed and accuracy. In contrary to the models developed in [10, 22] where two switchable voltage sources are required for the FB stack in each arm, only one controlled voltage source is required in the proposed model thus avoiding the switching between the two sources in [10, 22] and leading to faster simulation speed. For the FB model, the devices required in the auxiliary circuits are reduced from 12 to 6 while retaining all the possible current paths as in a real MMC during both active control and blocking mode. The required integration to calculate the SM capacitor voltage is also reduced from N to one in the proposed model. Compared to the model in [10], the simulation speed is significantly improved and the CPU running time is reduced by a third for the tested 2-terminal HVDC-link which can provide significant benefit when studying large HVDC networks involving many converter stations.

The paper is organised as follows. In Section 2, the accelerated SFM for the hybrid MMC is proposed, where the auxiliary circuits and the equivalent switching functions in the blocking state of the converter are introduced to accurately represent the converter behaviour under various operating conditions, including DC faults. The operating logics of the auxiliary circuits in the proposed model are described in Section 3. The proposed SFM of the hybrid MMC is assessed in Section 4, considering normal operation, AC fault, and DC fault in a point-to-point HVDC link. Finally Section 5 draws the conclusions.

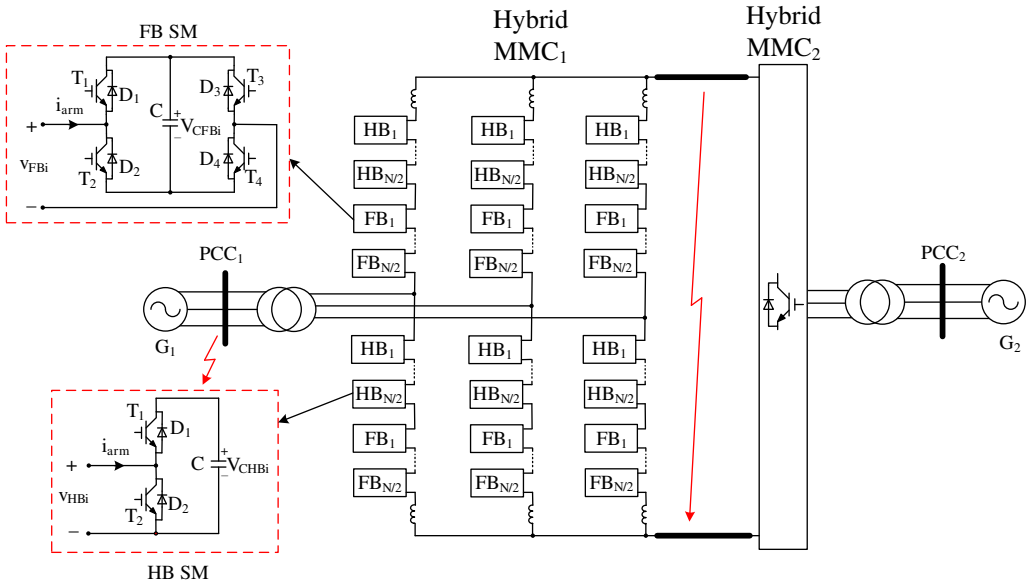


Fig. 1. Point-to-point HVDC link with hybrid MMCs

2. Accelerated Switching Function Model of Hybrid MMCs

By combining FB and HB SMs in each arm, the hybrid MMC as shown in Fig. 1 is capable of blocking a DC fault and is an attractive option for HVDC application [22, 24]. By introducing the switching functions in active control and blocking states, the SFM of hybrid MMC is derived in this section.

2.1. Switching Functions of the FB and HB SMs

2.1.1. During Actively Control of the Hybrid MMC

During active control (not blocked), each FB and HB SM can generate three and two voltage levels respectively, and thus their switching functions are defined as:

$$s_{FBi}=\begin{cases}0, & (T_1,T_3:\text{on};\ T_2,T_4:\text{off})\ \text{or}\ (T_2,T_4:\text{on};\ T_1,T_3:\text{off})\\ 1, & (T_1,T_4:\text{on};\ T_2,T_3:\text{off})\\ -1, & (T_2,T_3:\text{on};\ T_1,T_4:\text{off})\end{cases} \quad (1)$$

$$s_{HBi}=\begin{cases}0, & (T_2:\text{on};\ T_1:\text{off})\\ 1, & (T_1:\text{on};\ T_2:\text{off})\end{cases} \quad (2)$$

where s_{FBi} and s_{HBi} are the switching functions of the i^{th} FB and HB SMs, respectively; and the subscripts FB and HB denote the FB and HB SMs respectively.

From the switching functions defined by (1) and (2), each SM capacitor voltage of the proposed SFM can be calculated. Base on the trapezoidal integration, the current capacitor voltages $V_{CFBi}(t)$ and $V_{CHBi}(t)$ for the FB and HB stacks are obtained by adding the capacitor voltage variation $\Delta V_C(t)$ to the previous value $V_{CFBi}(t-\Delta t)$ and $V_{CHBi}(t-\Delta t)$, considering the switching function s_{FBi} and s_{HBi}:

$$V_{CFBi}(t)=V_{CFBi}(t-\Delta t)+s_{FBi}\cdot\Delta V_C(t). \quad (3)$$

$$V_{CHBi}(t)=V_{CHBi}(t-\Delta t)+s_{HBi}\cdot\Delta V_C(t). \quad (4)$$

In each arm, the FB and HB SM capacitors in the current path are charged or discharged by the same arm current, and thus have the same capacitor voltage variation $\Delta V_C(t)$:

$$\Delta V_C(t)=\frac{1}{C}\frac{i_{arm}(t)+i_{arm}(t-\Delta t)}{2}\Delta t \quad (5)$$

where C is the SM capacitance and Δt is the simulation step.

The total switching function s_{total} is obtained by rounding the product of the arm modulation index m_{arm} and the SM number per arm N:

$$\begin{aligned}s_{total}&=\sum_{i=1}^{N_{FB}}s_{FBi}+\sum_{i=1}^{N_{HB}}s_{HBi}=\text{round}(Nm_{arm})\\&=\text{round}\left[(N_{FB}+N_{HB})m_{arm}\right]\end{aligned} \quad (6)$$

where N_{FB} and N_{HB} are the respective FB and HB SM numbers per arm. Equation (6) determines the SM number inserted into the current path and discretizes the arm voltage of the SFM.

In the event of a pole-to-pole DC fault at the HVDC network, the DC voltage drops to almost zero. In order to operate the hybrid MMC on STATCOM mode, the required m_{arm} and s_{total} as shown in (6) could be less than zero. This indicates the FB SMs need to be inserted in the current path in negative polarity. The negative voltage generating capability of the hybrid MMC can be accurately reproduced by the proposed model, as will be discussed in Section 3.2.

2.1.2. In Blocking State of the Hybrid MMC

Alternatively, the hybrid MMC can be blocked during a DC fault. Immediately following the blocking of the MMC after the DC fault, the existing fault current in the arm charges the FB SM capacitors for both current directions as illustrated in Fig. 2 (a1) and (b1). In contrast, as shown in Fig. 2 (a2) and (b2), the HB SM capacitors are only charged by the positive arm current while the negative arm current flows through the antiparallel diode D_2, where positive arm current i_{arm} is defined as flowing from the top to the bottom.

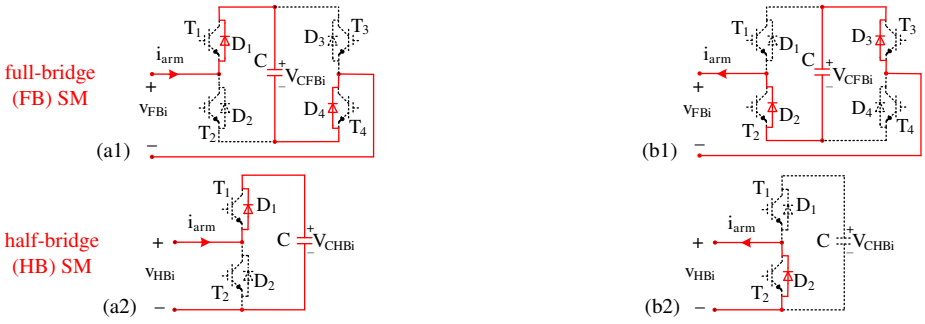


Fig. 2. Fault current path after the SMs are blocked, where the arm current i_{arm} flowing from the top to the bottom is defined as positive
a Positive arm current
b Negative arm current

After the SMs are blocked, the arm currents may charge the SM capacitors, as illustrated in Fig. 2. The proposed model calculates the capacitor voltages of each SM according to (3) and (4) where the switching function is considered. When the hybrid MMC is blocked, the firing pulses of all the IGBTs in the SMs are set at zero. Therefore, the aforementioned potential charging of the SM capacitors in blocking state cannot be represented and the capacitor voltages would remain unchanged if all the switching functions s_{FBi} and s_{HBi} in the blocking state are simply set as zero. To consider the potential

charging, equivalent switching functions in blocking state are defined to accurately calculate the SM capacitor voltage using (3) and (4) as:

$$s_{FBi}=\begin{cases}1, & (T_1,T_2,T_3,T_4:\text{off}) \ \& \ (i_{arm}\geq 0)\\ -1, & (T_1,T_2,T_3,T_4:\text{off}) \ \& \ (i_{arm}<0)\end{cases} \quad (7)$$

$$s_{HBi}=\begin{cases}1, & (T_1,T_2:\text{off}) \ \& \ (i_{arm}\geq 0)\\ 0, & (T_1,T_2:\text{off}) \ \& \ (i_{arm}<0)\end{cases}. \quad (8)$$

By considering the equivalent switching function, the potential charging of the SM capacitors during the blocking states is fully represented. Thus, the proposed SFM can precisely represent the SM capacitor voltage variations. This significantly improves the model accuracy compared to other alternatives, as will be demonstrated in Section 4.3.

2.2. Semiconductor Forward Voltage Drop of the SMs

The resistance of the off-state IGBT/diode R_{off} is very high and is normally in the range of several hundreds kΩ [3]. Table 1 lists the parameters of a 4.5kV/1200A IGBT from MITSUBISHI ELECTRIC [25]. The equivalent internal resistances (R_{onIGBT} and R_{onD}) and threshold voltages (V_{0IGBT} and V_{0diode}) are derived by linearizing the on-state characteristic curves provided in the datasheets.

Table 1 Typical parameters of a 4.5kV/1200A IGBT for HVDC application

PARAMETER		Value
IGBT	internal resistance R_{onIGBT}	1.8mΩ
	threshold voltage V_{0IGBT}	1.6V
Diode	internal resistance R_{onD}	0.9mΩ
	threshold voltage V_{0diode}	1.2V
Off-state resistance R_{off}		280kΩ

With the off-state IGBT considered as an open circuit (R_{off}=infinite), the semiconductor forward voltage drop of the SMs can be easily derived. The exact IGBT or anti-parallel diode which carries the arm current depends on the arm current polarity and the SM output voltage level. For the i^{th} FB and HB SMs, the forward voltage drops V_{fdFBi} and V_{fdHBi} are calculated as

$$V_{fdFBi}=\begin{cases}2R_{onD}i_{arm}(t)+2V_{0D}, & s_{FBi}=1,\ i_{arm}(t)\geq 0\\ 2R_{onIGBT}i_{arm}(t)-2V_{0IGBT}, & s_{FBi}=1,\ i_{arm}(t)<0\\ (R_{onD}+R_{onIGBT})i_{arm}(t)+V_{0D}+V_{0IGBT}, & s_{FBi}=0,\ i_{arm}(t)\geq 0\\ (R_{onD}+R_{onIGBT})i_{arm}(t)-V_{0D}-V_{0IGBT}, & s_{FBi}=0,\ i_{arm}(t)<0\\ 2R_{onIGBT}i_{arm}(t)+2V_{0IGBT}, & s_{FBi}=-1,\ i_{arm}(t)\geq 0\\ 2R_{onD}i_{arm}(t)-2V_{0D}, & s_{FBi}=-1,\ i_{arm}(t)<0\end{cases} \quad (9)$$

$$V_{fdHBi}=\begin{cases}R_{onD}i_{arm}(t)+V_{0D}, & s_{HBi}=1,\ i_{arm}(t)\geq 0\\ R_{onIGBT}i_{arm}(t)-V_{0IGBT}, & s_{HBi}=1,\ i_{arm}(t)<0\\ R_{onIGBT}i_{arm}(t)+V_{0IGBT}, & s_{HBi}=0,\ i_{arm}(t)\geq 0\\ R_{onD}i_{arm}(t)-V_{0D}, & s_{HBi}=0,\ i_{arm}(t)<0\end{cases}. \quad (10)$$

By considering the actual conducting semiconductor devices, their forward voltage drops are more accurately reproduced by (9) and (10).

2.3. Generated Arm Voltage in the Proposed SFM

When the hybrid MMC is actively controlled, the voltage v_{FB} and v_{HB} generated by the FB and HB stacks in the proposed model are then derived from the aforementioned switching functions, SM capacitor voltages, and semiconductor forward voltage drops:

$$v_{FB}=\sum_{i=1}^{N_{FB}}v_{FBi}=\sum_{i=1}^{N_{FB}}\left(s_{FBi}V_{CFBi}+V_{fdFBi}\right) \quad (11)$$

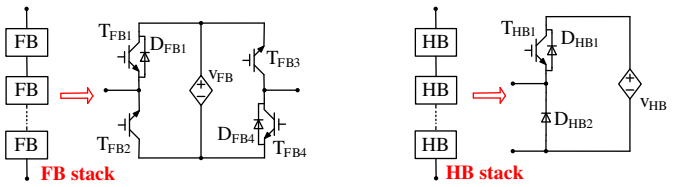
$$v_{HB}=\sum_{i=1}^{N_{HB}}v_{HBi}=\sum_{i=1}^{N_{HB}}\left(s_{HBi}V_{CHBi}+V_{fdHBi}\right) \quad (12)$$

where v_{FBi} and V_{CFBi} are the output and SM capacitor voltages of the i^{th} FB SM, respectively; v_{HBi} and V_{CHBi} are the output and capacitor voltages of the i^{th} HB SM, respectively. During active control of the hybrid MMC, the contribution of the SM capacitor voltages V_{CHBi} and V_{CFBi} to v_{FB} and v_{HB} depends on the switching functions s_{FBi} and s_{HBi}. When the hybrid MMC is blocked, the reference voltages v_{FB} and v_{HB} are independent to the equivalent switching functions defined in (7) and (8) and all the FB and HB SM capacitor voltages V_{CHBi} and V_{CFBi} are added to v_{FB} and v_{HB} respectively:

$$v_{FB}=\sum_{i=1}^{N_{FB}}v_{FBi}=\sum_{i=1}^{N_{FB}}\left(V_{CFBi}+V_{fdFBi}\right) \quad (13)$$

$$v_{HB}=\sum_{i=1}^{N_{HB}}v_{HBi}=\sum_{i=1}^{N_{HB}}\left(V_{CHBi}+V_{fdHBi}\right). \quad (14)$$

3. Operating Logics of the Auxiliary Circuits in the Proposed SFM



a b

Fig. 3. Proposed switching function models for
a Series-connected FB stack in each arm
b Series-connected HB stack in each arm

In each arm of the MMC, each of the FB and HB stacks, which are composed of hundreds SMs connected in-series, are represented by equivalent voltage sources v_{FB} and v_{HB} connected with the auxiliary circuit in the proposed model, as illustrated in Fig. 3, to simulate the current path in normal operation and during faults. The auxiliary circuit is composed

of IGBTs T_{FB1}-T_{FB4} and diodes D_{FB1} and D_{FB4} for the FB stack model; and IGBTs T_{HB1} and diodes D_{HB1} and D_{HB2} for the HB stack model, as shown in Fig. 3 (a) and (b) respectively. The switching logics of the auxiliary circuit will be discussed in this section.

3.1. Switching Logics of the Auxiliary Circuit in the Proposed SFM for HB Stack

The switching function model of the HB stack is derived from the AMs in [7] and [22] but has the capability of representing the voltages of each SM capacitor. As the HB SMs do not generate negative voltage, the voltage v_{HB} produced by the HB SM stack, in Fig. 3 (b), is always greater than or equal to zero. The switching logics of the auxiliary circuit in the SFM for HB stack is governed by

$$\begin{cases} T_{HB1}: \text{on} & \text{during active control} \\ T_{HB1}: \text{off}, & \text{in blocking state} \end{cases}. \quad (15)$$

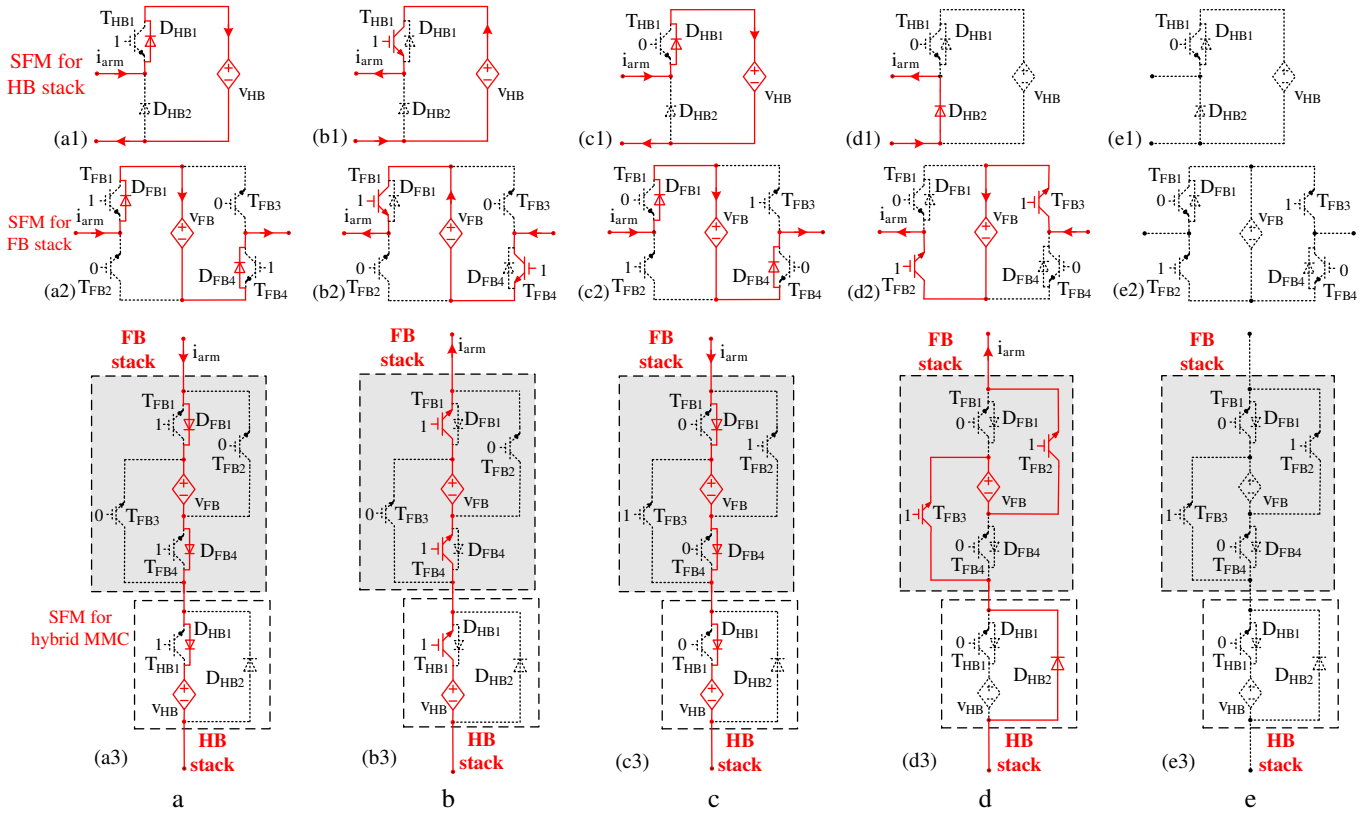


Fig. 4. Arm current paths of the proposed SFM for HB stack, FB stack, and hybrid MMC in each arm respectively
a Actively controlled with positive arm current
b Actively controlled with negative arm current
c Blocking state with positive fault current
d Blocking state with negative fault current
e High impedance state

When the converter is actively controlled, the IGBT T_{HB1} for the HB stack in Fig. 3 (b) is always on, allowing the arm current to flow in both positive and negative directions through the IGBT T_{HB1} or its antiparallel diode D_{HB1}, as shown in Figs. 4 (a1) and (b1) respectively, while diode D_{HB2} is reverse biased.

As the HB SMs do not have DC fault blocking capability, the fault current from the AC grid flows through the SM antiparallel diodes (negative arm current) into the DC fault after the blocking of the MMC. This is represented by turning off the IGBT T_{HB1} and the fault current is allowed to flow through diode D_{HB2} from the AC to the DC side, Fig. 4 (d1). As shown in Fig. 4 (c1), the positive fault current flows through the antiparallel diode D_{HB1} and charges the voltage source v_{HB}, which can be depicted by (4) and (8). This is identical to the current path when the converter is actively controlled with positive arm current, Fig. 4 (a1), although they have opposite switching logics for the auxiliary circuit.

3.2. Switching Logics of the Auxiliary Circuit in the Proposed SFM for FB Stack

From the model of the HB SM stack shown in Fig. 3 (b), an alternative model for the FB stack is derived, as illustrated in Fig. 5 (a), which can represent the behaviour of the FB stack, except the negative voltage generating capability during active control. To continuously operate the hybrid MMC in STATCOM mode under a DC fault, the FB stack needs to generate negative voltage. Thus, the generated voltage v_{FB} in

the proposed SFM for FB stack can be less than zero. This results in the shoot-through of the diode pairs (D_{FB1}, D_{FB2}) and (D_{FB3}, D_{FB4}) for $v_{FB} < 0$, as shown in Fig. 5 (b), where the shoot-through currents i_{st1} and i_{st2} are illustrated.

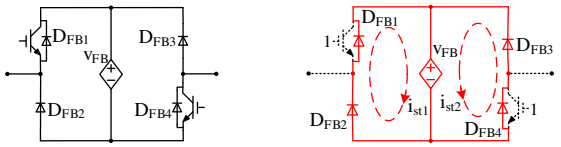


Fig. 5. Alternative model without negative voltage representation
a Model for the FB stack in each arm
b Shoot-through of diode pairs (D_{FB1}, D_{FB2}) and (D_{FB3}, D_{FB4}) when v_{FB} is negative

To avoid diode shoot-through, diodes D_{FB2} and D_{FB3} are replaced by IGBTs T_{FB2} and T_{FB3} in the proposed model, as shown in Fig. 3 (a). T_{FB2} and T_{FB3} act in the manner similar to ideal switches used in the MMC modeling in [9, 10], but with unidirectional current flow. The IGBT switching logics of the proposed model for FB stack are

$$\begin{cases} (T_{FB1}, T_{FB4}): \text{on}, \quad (T_{FB2}, T_{FB3}): \text{off}, & \text{during active control} \\ (T_{FB1}, T_{FB4}): \text{off}, \quad (T_{FB2}, T_{FB3}): \text{on}, & \text{in blocking state} \end{cases} \quad (16)$$

When the MMCs are actively controlled (not blocked), the switches T_{FB1} and T_{FB4} are always on while T_{FB2} and T_{FB3} are turned off. Thus the arm currents can flow in both positive and negative directions through the antiparallel diodes D_{FB1} and D_{FB4} or the IGBTs T_{FB1} and T_{FB4}, as illustrated in Figs. 4 (a2) and (b2). The voltage stresses on IGBTs T_{FB1} and T_{FB4} are zero, and T_{FB2} and T_{FB3} support the voltage v_{FB} with both positive and negative polarities. The shoot-through issue illustrated in Fig. 5 (b) is thus avoided. The negative voltage capability of the proposed model, thereby the continuous operation in STATCOM mode, will be presented in Section 4.3.

The blocking of the MMCs after a fault is represented by turning off the IGBTs T_{FB1} and T_{FB4} and activating T_{FB2} and T_{FB3} in the proposed model. The positive fault current flows through the antiparallel diodes D_{FB1} and D_{FB4} and charges the equivalent voltage source v_{FB}, as shown in Fig. 4 (c2). Although the switching logics for the auxiliary circuit are opposite, the current path in Fig. 4 (c2) is identical to that in Fig. 4 (a2). In Fig. 4 (d2), the negative fault current also charges the voltage source v_{FB} through T_{FB2} and T_{FB3} and gradually drops. After the fault currents are suppressed to around zero (only leakage currents exist), the system operates in the high impedance mode [26, 27], as illustrated in Fig. 4 (e2) (none of the devices are ON).

The proposed model provides all the possible current paths as in a real MMC during active control and blocking mode and thus can be used to analyze the MMC behaviour under fault conditions.

3.3. Proposed SFM for the Hybrid MMC

Combining the SFMs for FB and HB stacks, the current paths for each arm of the hybrid MMC are shown in Figs. 4 (a3-e3). From (11) and (12), the generated arm voltages of the hybrid MMC, v_{arm}, during active control and in the blocking state are

$$v_{arm} = v_{FB} + v_{HB} = \sum_{i=1}^{N_{FB}} \left(s_{FBi} V_{CFBi} + V_{fdFBi} \right) + \sum_{i=1}^{N_{HB}} \left(s_{HBi} V_{CHBi} + V_{fdHBi} \right) \quad (17)$$

$$v_{arm} = v_{FB} + v_{HB} = \sum_{i=1}^{N_{FB}} \left(V_{CFBi} + V_{fdFBi} \right) + \sum_{i=1}^{N_{HB}} \left(V_{CHBi} + V_{fdHBi} \right). \quad (18)$$

As aforementioned, both the internal resistance and threshold voltage of the semiconductors in each SM are considered when calculating the reference voltages v_{FB} and v_{HB}, as depicted by (9) and (10). Thus, these parasitic parameters of the IGBTs and diodes in the auxiliary circuit do not need to be considered again, i.e. IGBTs T_{HB1} and T_{FB1}-T_{FB4}, and diodes D_{HB1}, D_{HB2}, D_{FB1}, and D_{FB4} are set in the manner similar to ideal devices.

In the simulation platform of the MATLAB/Simulink, snubber circuits are usually connected to the semiconductor devices in parallel to avoid spikes during switching transients. A pure resistive snubber circuit is adopted for the IGBTs and diodes in the auxiliary circuit (T_{FB1}-T_{FB4}, T_{HB1}, D_{FB1}, D_{FB4}, D_{HB1}, and D_{HB2}) where the snubber resistance R_s is properly set to represent the high impedance state of the SMs in the hybrid MMC, as:

$$R_s = \tfrac{1}{2} R_{off} N. \quad (19)$$

With the off-state resistance R_{off} of 280kΩ as listed in Table 1, the peak of the leakage arm current for the simulated full-scale HVDC link (with the parameters detailed in Table 2) is around 10mA which is represented by the snubber circuit in the proposed MMC model.

Table 2 Nominal parameters of the test full-scale HVDC link in Fig. 1

PARAMETER	Nominal Value
DC voltage	±400kV
power rating	1200MW
grid- and converter-side voltage of the interface transformer	400kV/345kV
SM number per arm N	**320**
SM capacitance	7.9mF
SM capacitor voltage	2.5kV
arm inductance	30mH (0.1p.u.)
pi section number of DC cable	10
length of DC cable	100km
R, L and C of DC cable	12mΩ/km, 0.8mH/km, 0.21μF/km

As discussed in [26], the numerical oscillation only exists in the hard coded model (Model 2) which uses written codes to depict the complicated conduction and blocking states

of diodes. Such issue is not reported for the models which use IGBTs/diodes to reproduce the fault current paths [10, 26]. Similarly, the potential conduction of diodes in blocking state is implemented using auxiliary circuits in the proposed model, avoiding the numerical oscillation problems seen in Model 2 in [26]. In addition, as presented in [26], the simulation speed of the hard coded model (Mode 2) is slower than Mode 3 which also adopts diodes to represent the fault current paths, due to the complicated codes of Mode 2.

4. Validation of the Proposed SFM

The presented SFM for hybrid MMC is assessed using the point-to-point HVDC link shown in Fig. 1. The simulation tool for this study is the Simscape/SimPowerSystems in the R2016a 64-bit MATLAB/Simulink® environment. The down-scale 25-level (24 SMs per arm), 40MW / ±12kV system with parameters listed in Table 3 is simulated using both detailed switching model and the proposed SFM for accuracy and simulation speed validation. A full-scale 321-level system with parameters listed in Table 2 is also simulated. The HB and FB SM numbers N_{FB} and N_{HB} are both set at N/2 to successfully block the DC fault.

Table 3 Nominal parameters of the test down-scale HVDC link in Fig. 1

PARAMETER	Nominal Value
DC voltage	±12kV
power rating	40MW
grid- and converter-side voltage of the interface transformer	16kV/13.2kV
SM number per arm N	**24**
SM capacitance	22.2mF
SM capacitor voltage	1kV
arm inductance	1.4mH (0.1p.u.)
pi section number of DC cable	10
length of DC cable	10km
R, L and C of DC cable	5mΩ/km, 0.2mH/km, 0.22μF/km

The arm inductance is set at 0.1p.u. to limit the circulating currents and the fault current rising rate [28, 29]. The IGBTs rated at 4.5kV are normally operated at around 2.5kV in HVDC application and thus 320 SMs are required per arm for the full-scale ±400kV HVDC system [25, 30]. The AC voltage rating of 400kV is standard for the high voltage grid in the UK and is thus adopted in this paper [31]. The DC cable parameters are based on the datasheets of cable manufacturers (ABB [32] and NKT Cables [33]) and the literatures of [30, 34].

4.1. Pre-charging of Hybrid MMC using the Down-scale System

The blocking state of the hybrid MMC is tested in the uncontrolled pre-charging scenario first, where all the SM capacitor voltages are initially set at zero and the hybrid MMC is blocked. To limit inrush currents, as a common practice, resistors of 3Ω are inserted between the transformer and the converter. Fig. 6 compares the simulated pre-charging process for the DSM and SFM using the down-scale 25-level system.

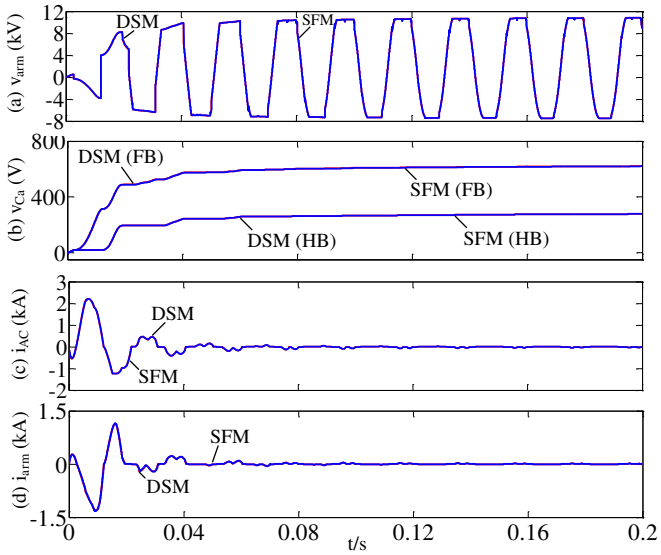


Fig. 6. Comparison of the pre-charging of the hybrid MMC with 25 levels using DSM and SFM
a Arm voltages
b FB and HB SM capacitor voltages
c AC currents
d Arm currents

In addition to the positive voltage, the hybrid MMC arm also produces negative voltage during the uncontrolled charging process depending on the current direction of the FB SMs, Fig. 6 (a). The FB SM capacitors are charged by both positive and negative currents whereas the HB SM capacitors can only be charged by positive currents and are bypassed when the arm currents are negative. This leads to imbalanced charging between the FB and HB SM capacitors, as shown in Fig. 6 (b). The sequentially controlled charging method presented in [35] could be used to achieve equal charging of capacitors for the hybrid MMC. Nevertheless, the results of the proposed model match that of the detailed switching model (with almost identical results) and the uncontrolled charging process of the hybrid MMC is accurately represented by the SFM, as displayed in Fig. 6.

4.2. Startup of Hybrid MMC using the Full-scale System

The performance of the proposed SFM is also assessed using the aforementioned full-scale system with 321-level hybrid MMCs. For illustration purpose, all the capacitor voltages are initially set at the rated value and the active power is fast ramped from zero to 1p.u. in the duration of (0-0.1s). Close match is observed in Fig. 7 and the proposed model can reproduce the startup process of the hybrid MMC.

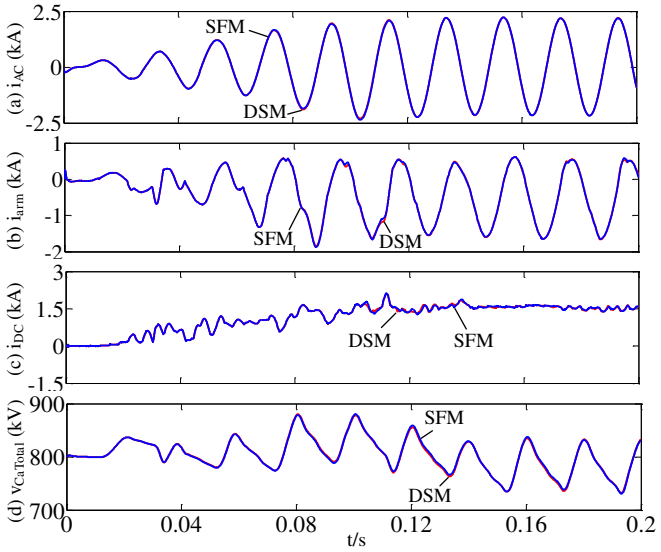


Fig. 7. Comparison of the startup of the hybrid MMC with 321 levels using DSM and SFM
a AC currents
b Arm currents
c DC currents
d Total capacitor voltages in an arm

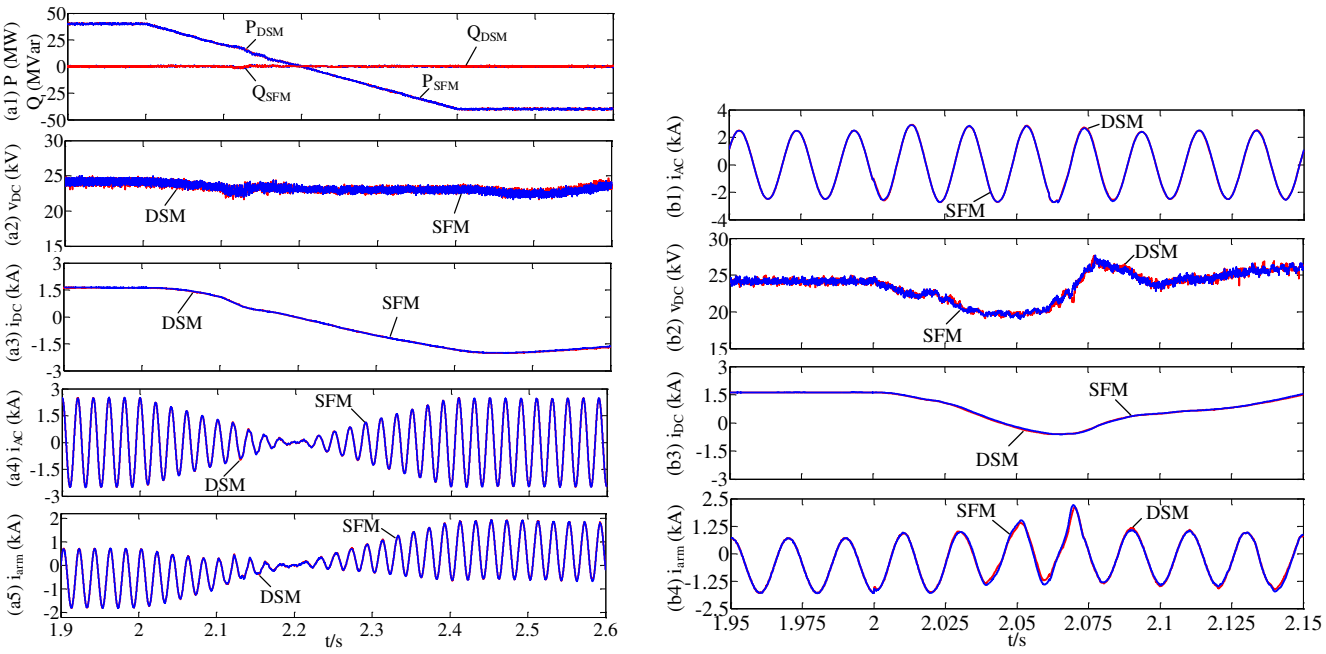
4.3. Normal Operation using the Down-scale System

In this simulation, the hybrid MMC_2 regulates the DC voltage while MMC_1 initially imports the rated 40 MW power from G_1 to the DC link with unity power factor. During t=2-2.4s, the power flow direction is reversed with the change rate of active power being -200MW/s. The comparison between the detailed switching model and the proposed model is presented in Fig. 8 (a), where close match is observed for all the waveforms. This validates that the proposed SFM can fully reproduce the dynamic behaviour of the hybrid MMC during power reversal.

4.4. AC Fault Scenario using the Down-scale System

The simulated scenario assumes a temporary three-phase-to-ground fault is applied on the AC-side of hybrid MMC_1, as shown in Fig. 1, at t_0=2s and is cleared after 60ms. Both stations keep operating during the AC fault.

Fig. 8 (b) compares the detailed switching model and the proposed SFM for the down-scale HVDC link. It can be seen that the proposed model again provides a highly accurate representation of the transients of the hybrid MMC during the AC fault.



a b

Fig. 8. Waveform comparison between the proposed SFM and the DSM
a During power reversal initiated at t_0=2s: (a1) active and reactive power, (a2) DC voltages, (a3) DC currents, (a4) AC currents, and (a5) arm currents
b Under a three-phase-to-ground fault occurred at t_0=2s: (b1) AC currents, (b2) DC voltages, (b3) DC currents, and (b4) arm currents

4.5. DC Fault Operating Condition

After the DC fault, the hybrid MMC can be deactivated to block the fault. Alternatively, the hybrid MMC can also continue operating during the fault as the FB SMs can generate negative voltages. These two operations will be assessed in this subsection using the proposed SFM to validate its effectiveness for the DC fault studies.

4.5.1. *Blocking the Hybrid MMC during the Fault using the Down-scale System*

After the fault detection, the converters are blocked. The FB SM capacitors are then charged by both positive and negative arm currents while the HB SM capacitors are only charged by the positive arm current (from the top to the bottom), as previously shown in Figs. 4 (c3) and (d3). Due to the introduction of the equivalent switching functions (equation (7) and (8)) in the proposed SFM after the MMC is blocked, the potential charging of the capacitors for both the FB and HB SMs are accurately represented.

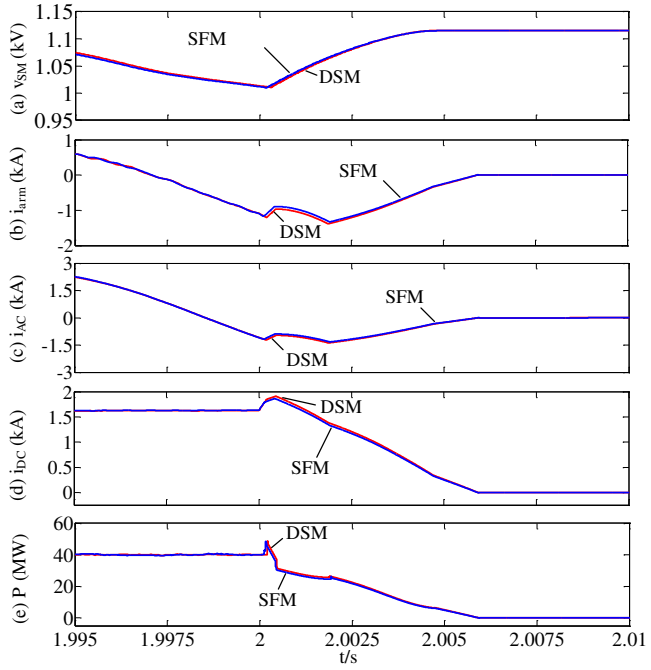


Fig. 9. Comparison between the proposed SFM and the DSM, where the pole-to-pole DC fault occurs at t_0=2s and the MMC is blocked after the fault
a Average SM capacitor voltages
b Arm currents
c AC currents
d DC currents
e Active power

Fig. 9 (a) compares the proposed SFM and the DSM for the down-scale 25-level HVDC link. The system is subjected to a permanent pole-to-pole DC fault at the middle of the DC cable at t_0=2s and the hybrid MMCs are blocked after fault detection. As demonstrated in Fig. 9 (a), the waveforms of the proposed model match that of the detailed model before and after the blocking of the converter.

4.5.2. *Continuous Operation of the Hybrid MMC during the DC Fault using the Full-scale System*

The proposed SFM during continuous operation is assessed using the full-scale 321-level HVDC system with the parameters listed in Table 2. In the pre-fault condition, hybrid MMC_1 imports 540MW active power from G_1 and exchanges 430MVar (inductive) at its AC side with G_1, while MMC_2 is set to maintain the DC voltage constant at ±400kV. The DC fault occurs at t_0=2s and the converter continues operating and provides reactive support for the AC grid.

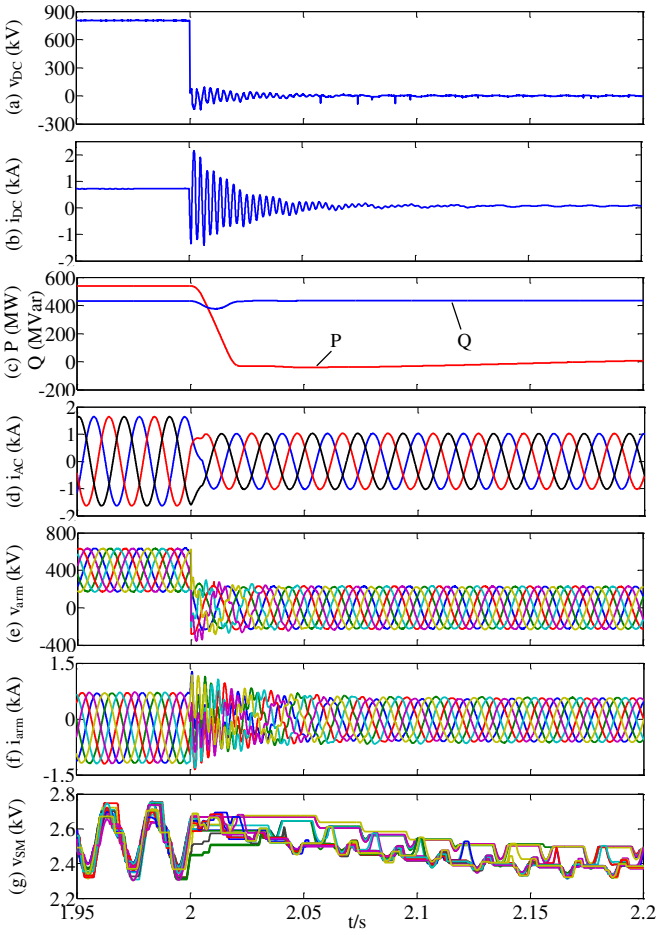


Fig. 10. Waveforms of the proposed SFM for the 321-level hybrid MMC, where the pole-to-pole DC fault occurs at t_0=2s and the MMC remains operational after the fault
a DC voltage
b DC current
c Active and reactive power
d AC currents
e Arm voltages
f Arm currents
g SM capacitor voltages

As the FB SMs have negative voltage generating capability, Fig. 10 (e), the hybrid MMC keeps operating although the DC voltage drops to around zero, Fig. 10 (a). Thus, the reactive power change between the AC and DC sides is controlled while the active power is decreased to zero (STATCOM mode), Fig. 10 (c). The AC side currents are also well regulated and the arm currents only experience small disturbance, as displayed in Fig. 10 (d) and (f). The proposed model can reproduce the capacitor voltage variation of each SM for the full-scale hybrid MMC with hundreds of SMs per arm, as shown in Fig. 10 (g). With the sorting algorithm presented in [36-38], the SM capacitor voltages are balanced during the ride-though operation and there are no extra requirements for the SM capacitor voltage balancing in the continuous operation of the hybrid MMC during a DC fault.

The proposed SFM is capable of simulating high frequency behaviour during a fault and obtain satisfactory simulation accuracy. This is achieved with the typical SM capacitance requirement of 30-40kJ/MVA as suggested by ABB in [39], which yields a capacitor voltage ripple in the range of ±10% [40-44], as shown in Fig. 10 (g) . In contrast,

the average model in [2] is only valid when the SM capacitance is large enough to maintain near constant SM capacitor voltage. According to the switching function, the capacitor voltages of all the SMs are considered in the proposed SFM, as shown in Fig. 10 (g), leading to higher simulation accuracy.

Table 4 Simulation speed comparison of the proposed SFM and other alternatives

Output Phase Voltage Level	Running Time (s)		
	DSM	Model in [10]	Proposed SFM
25	1,021	26	22
321	282,780 (estimated)	65	41

4.6. Simulation Speed Comparison

In addition to the higher accuracy, the proposed SFMs for hybrid MMC significantly accelerate the simulation speed. Two seconds of simulation is simulated in the MATLAB/Simulink® software package with a simulation step of 5µs, based on the Microsoft Windows 7 Enterprise platform with Intel Core i7 CPU @3.4GHz and 16GB RAM. For the down-scale 25-level HVDC link, the running time is significantly reduced from 1021s for DSM to 22s for the proposed SFM, as listed in Table 4. For the full-scale 321-level system the running time is only 41s for a 2s simulation. As it is extremely time consuming to simulate the full DSM with 321-levels, only a very short simulation (0.2s) is conducted. Scaling the implemented simulation time to the expected time of 2s, the estimated running time of the detailed switching mode with 321-levels is over 78 hours. For the hybrid MMC with 25 levels, the proposed SFM has close run time with the model in [10], (22s and 26s respectively, Table 4). However, the proposed model is much faster than the model in [10] to simulate the system with 321 levels and the run time is significantly reduced by a third (from 65s to 41s) which can provide significant benefit when studying large HVDC networks involving many converter stations.

5. Conclusion

This paper proposes an accelerated switching function model (SFM) for the hybrid MMC, where auxiliary circuits are adopted to represent all the possible current paths. The proposed SFM can represent the negative voltage generating capability of the FB stack while avoids the shoot-through of the diodes. In addition, the switching functions of the FB and HB SM in the blocking states are introduced in the proposed SFMs to depict the potential charging of the SM capacitors by the fault current, after the MMCs are blocked. Thus, the proposed model accurately replicates the capacitor voltage variations of each SM, which significantly improves the model accuracy and simulation speed when compared to other existing models. Simulation results validate that the proposed SFM of the hybrid MMC can provide accurate representation of MMC behaviour during various operating conditions, including normal operation, AC fault, and DC fault, etc.

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